

**REMARKS**

Claim 1 has been amended to better define the claimed invention. No new matter has been entered by any of the foregoing amendments.

The art rejections are respectfully traversed.

Considering first the rejection of claims 1 and 2 under 35 USC §102(b) as being anticipated by U.S. Patent No. 4,682,200 to Uchida et al., Uchida et al. does not teach setting the gate length longer than a half pitch, i.e., the minimum processing dimension, as required by claim 1. Instead, Uchida et al. merely teaches setting the gate length longer than 2 $\mu$ m (Column 12, lines 5-7). The Uchida et al reference teaches setting the gate length longer than some absolute length, but does not teach the length of the gate electrode in relation to the half pitch. Thus, claim 1 and claim 2 which depends thereon cannot be said to be anticipated by Uchida et al.

The rejection of claims 1-3, 8, and 18 under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,426,175 to Furukawa et al. likewise is in error. Furukawa et al. fails to disclose a gate length of said gate electrode is longer than a half pitch as required by independent claims 1 and 18. The Examiner states on page 3 of the office action that Furukawa et al. teaches "a gate length of said gate electrode is longer than a half pitch (or minimum processing dimension F)." However, what Furukawa et al. teaches is a unit F that is neither defined as a half pitch nor as a minimum processing dimension. Rather, Furukawa et al, at col. 15, lines 54-58, teaches F is a lithographic unit, specifically a minimum feature size for conventional photolithography. Further to this point, at the passage called out in the office action, Furukawa et al. teaches processing elements of a cell smaller than F. By definition, elements cannot be processed at a size below a

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minimum processing dimension. Thus, claim 1 and claims 2, 3 and 8 which depend thereon, and claim 18 cannot be said to be obvious from Furukawa et al.

The rejection of claims 1 and 2 under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,396,096 to Park et al. also is in error. The passage of Park et al. identified by the Examiner is utilizing a wiggled wordline. The wiggle in the wordline causes the gate length in some portions to be greater than 1F and in other portions no greater than 1F (see col. 4, lines 13-23). Claim 1 requires a minimum gate length being greater than 1F. Since the wordline of the present invention is without wiggle and is identified as having a gate length of greater than 1F, claim 1 and claim 2 which depends thereon cannot be said to be anticipated by Park et al.

The rejection of claims 4-6 under 35 USC §103(a) as being unpatentable over Park et al. in view of Applicants admitted prior art also is in error. Claims 4-6 depend, indirectly, on claim 1. The deficiencies of Park et al. vis a vis claim 1 are discussed above. Claims 4-6 are allowable for the same reasons above adduced relative to claim 1, as well as for their own additional limitations.

Finally, and with reference to the rejection of claim 7 under 35 USC §103(a) as being unpatentable over Furukawa et al., claim 7 is dependent on claim 1. The deficiencies of Furukawa et al. vis a vis claim 1 are discussed above. Claim 7 is similarly allowable for the same reasons above adduced relative to claim 1 as well as for its own additional limitations.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

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Respectfully submitted,



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